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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,198	04/20/2004	Ying-Yao Lin	REAP0009USA4	3197

27765 7590 06/14/2005

NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,198	LIN ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8 and 9* is/are rejected.

7)☒ Claim(s) *5-7 and 10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/20/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/709,198 filed on 02/26/04. Claims 1 – 12 are pending on this application.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Claim 2 and 3 are objected to the phrase "can be " renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Appropriate correction is required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1 – 3 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 2 of copending Application 10/709,198. Although the conflicting claims are not identical, they are not patentably distinct from each other because both invention having substantial the same subject matter for voltage gain is inversely in an exponential function; wherein the value of exponential function being determined by the difference between the first and second controlling voltage.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1 – 4, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Fritz U.S. patent No. 5,030,924.

Regarding claim 1, Fig. 1 and 2 of Fritz discloses a variable gain amplifier, comprising: an amplifying stage (Q5, Q6) for generating an output voltage (out+, out-) according to a differential input voltage (In+, In-); and a gain controlling stage (Fig. 2) for generating a gain controlling voltage (19, 21) to control a voltage gain (to VBQ7, to VBQ8) of the amplifying stage (Fig. 1) according to a first controlling voltage and a second controlling voltage (Fig. 2 [VBYB and BREF), such that the voltage gain is inversely proportional to a simple exponential function (Col. 6 line 20), the value of the simple exponential function being determined by the difference between the first controlling voltage and the second controlling voltage (Col. 6 line 15).

Regarding claim 2, wherein the denominator of the voltage gain of the amplifying stage can be expressed as (K1+exp(K2.times.Vy)), wherein both K1 and K2 are substantially constants and Vy is the gain controlling voltage (Col. 8 lines 50 – 53).

Regarding claim 3, wherein the gain controlling voltage can be expressed in the form of the difference of the first and the second controlling voltages (Col. 8 lines 50 – 53).

Regarding claim 4, wherein the gain controlling stage comprises: a transconductance unit (Q1, Q2) for generating a first current and a second Current (Ic of Q1, and Ic of Q2) according to the first controlling voltage (VBYP) and the second controlling voltage (VREF), wherein the ratio between the first current and the second current is determined by the difference between the first controlling voltage and the second controlling voltage (Col. 7 line 5 – 10); a current transforming unit (Q3, Q4) coupled to the transconductance unit (Q1, Q2) for generating a third current (Ic of Q4)

corresponding to the first current (Ic of Q1), and a fourth current (Ic of Q3) corresponding to the second current (Ic of Q2); and an outputting unit (See Fig. 1[Q7, Q8) connected to VBQ8, and VBQ7 of transformed unit)) coupled to the current transforming unit for generating the gain controlling voltage (Col. 6 line 1) according to the third current and the fourth current; wherein the value of the gain controlling voltage is determined by the difference between the first controlling voltage and the second controlling voltage (Col. 6 line 7).

Regarding claim 8, wherein the transconductance unit (Q1, Q2) comprises: a first transistor (Q1) coupled to the first controlling voltage (VBYP); a second transistor (Q2) coupled to the second controlling voltage (VREF); and a first bias current source (I1) coupled to the first transistor and the second transistor for providing a first bias current (I1); wherein the first transistor outputs the first current (Ic of Q1) according to the first controlling voltage (VBYP) and the first bias current (I1), and the second transistor outputs the second current (Ic of Q2) according to the second controlling voltage (VREF) and the first bias current (I1).

Regarding claim 9, wherein the outputting unit comprises: a third transistor (Q3) , wherein the current of the third transistor corresponds to the fourth current (Ic of Q3); a fourth transistor (Q4); and a second bias current source (I2) coupled to the third transistor and the fourth transistor for providing a second bias current (I2), wherein the second bias current corresponds to the third current (Ic of Q4); wherein the third transistor (Q3, Q4) and the fourth transistor are for outputting the gain controlling voltage.

Allowable Subject Matter

8. Claims 5 - 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. With respect to claim 5, the prior art does not teach or suggest wherein the relationship between the first current, the second current, the first controlling voltage, and the second controlling voltage is: I1/I2=exp(K.times.(V1-V2)-); where I1 is the first current, I2 is the second current, V1 is the first controlling voltage, and V2 is the second controlling voltage.

9. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or suggest wherein the value of the second bias current is substantially the same as the value of the third current, and the value of the current of the third transistor is substantially the same as the value of the fourth current.

10. Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or suggest wherein the current transforming unit comprises a current mirror circuit.

11. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or suggest wherein

the current transforming unit comprises: a first current transforming unit, comprising: a fifth transistor having a first end being coupled to a second end; a sixth transistor; a third bias current source coupled to a third end of the fifth transistor and the sixth transistor for providing a third bias current; and a fourth current source coupled to the fifth transistor and the transconductance unit; and a second current transforming unit comprising: a seventh transistor having a first end and a second end being coupled to the sixth transistor for outputting the third current; an eighth transistor coupled to the fifth transistor for outputting the fourth current; and a fourth bias current source coupled to the seventh transistor and the eighth transistor for providing a fourth bias current.

Prior Art

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are

(703-872-9306) for regular communications and (703-872-9306) for After Final communications.

6/6/05

Linh Van Nguyen

Art Unit 2819